UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/727,474 | 12/04/2003 | Carlo Grillettc | 03-1681 | 6257 |

24319 7590 12/15/2004

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

| EXAMINER | |
|---|---|
| NGUYEN, TUNG X | |
| **ART UNIT** | **PAPER NUMBER** |
| 2829 | |

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/727,474 | GRILLETTC, CARLO | |
| | Examiner | Art Unit | |
| | Tung X Nguyen | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9-11, 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeng et al. (u.s.p 6,287,878).

As to claims 1, 7, 9, Maeng et al. disclose in Fig. 3-11, a method of testing a subject integrated circuit package comprising: mounting the subject IC package (114 of figure 11) on a subject printed circuit board (PCB 154); removably connecting the subject PCB (154) to a motherboard (162) along with a plurality of other PCBs having other IC packages (114) mounted thereon; monitoring the subject IC package and the other IC packages for test failure during exposure to the thermally varying test conditions (col. 5, lines 10-15; and col. 6, lines 10-15); determining whether the subject IC package has experienced the test failure to remove the subject PCB from the motherboard (col. 5, lines 10-15, col. 6, lines 15-20); performing an electrical test on the subject IC package to determine a location of the test failure (col. 6, lines 10-20).

As to claim 2, Maeng et al. disclose in Fig. 11, removably connecting the subject PCB to the motherboard by edge card connection (via socket 164).

As to claim 3, Maeng et al. disclose in Fig. 11, the subject PCB (154) has edge card connectors on only one edge.

As to claim 4, Maeng et al. disclose in Fig. 11, removing the subject PCB (154) from the motherboard (162) without altering the motherboard.

As to claim 5, Maeng et al. disclose in Fig. 11, continuing the exposing and monitoring of the other IC packages and the other PCBs while electrically testing the subject IC package (col. 6, lines 15-20).

As to claim 6, Maeng et al. disclose in Fig. 11, returning the subject PCB to the motherboard to resume the exposing and monitoring of the subject IC package and the subject PCB (col. 6, lines 15-20).

As to claim 10, Maeng et al. disclose in Fig. 11, subjecting the motherboard, the PCBs and the IC packages to thermal and relative humidity test conditions (col. 6, lines 10-15).

As to claim 11, Maeng et al. disclose in Fig. 11, a highly accelerated stress test (col. 5, lines 11-14).

As to claim 18, Maeng et al. disclose in Fig. 3-11, an integrated circuit package testing apparatus comprising: a plurality of printed circuit boards (PCBs 154 of figure 11), each having edge connectors coupled to the motherboard (162 of figure 11); and each capable of supporting an IC package (114 of figure 11) to be tested; and the PCBs are removably connected to the motherboard; and wherein the motherboard, the PCBs and the IC packages are adapted to be subjected to electrical bias test signals (col. 6, lines 5-15); and the motherboard and the PCBs are adapted to be separated for electrical testing of the PCBs and the IC packages to determine whether the electrical

bias test signals caused a failure condition in any of the IC packages (col. 5, lines 10-15).

As to claim 19, Maeng et al. disclose in Fig. 11, the PCBs (154) are connected substantially perpendicular to the motherboard (162 of figure 11).

As to claim 20, Maeng et al. disclose in Fig. 11, the motherboard, the PCBs and the IC packages are adapted to be subjected to a highly accelerated stress test (col. 5, lines 5-15).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeng et al. (u.s.p 6,287,878), in view of Kiyokawa et al. (u.s.p 5,742,168).

As to claims 8, 12-13, Maeng et al. disclose in Figs. 3-11, an integrated circuit package testing apparatus comprising: a plurality of printed circuit boards (PCBs 154), each capable of supporting an IC package (114 of figure 11) to be tested; and a motherboard (162 of figure 11) to with the PCBs are removably connected (socket 164 of figure 11); and wherein the motherboard (162), the PCBs and the IC packages in the burn-in testing; an electrical test is performed simultaneously while stress for burn-in testing is being applied to the PCBs, and IC packages (col. 4, line 4-10); Then, an electrical signal are applied to the plurality of IC package inserting into PCBs(154) on

the motherboard (162) to monitor for a failure condition, therefore to determine a location of a cause of the failure condition (col. 5, lines 7-14).

Maeng et al does not disclose the IC package inserted into the PCBs on the motherboard placed in a thermal test chamber. However, Kiyokawa et al disclose in Fig. 4, the IC package inserted into the PCBs on the motherboard placed in a thermal test chamber (20 of fig. 4) for keeping the temperature constant during stress the electrical signal on the IC package (fig. 4). Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Maeng et al, and provides a thermal test chamber, as taught by Kiyokawa et al. for keeping the temperature constant during stress the electrical signal on the IC package (fig. 4).

As to claim 14, Maeng et al disclose in Fig. 11, the integrated circuit packages (114 of figure 11) coupled to the PCBs (154) are connected substantially perpendicular to the motherboard (162 of figure 11).

As to claim 15, Maeng et al. disclose in Fig. 11, the PCBs (154) have an edge card coupled to motherboard (via socket 164).

As to claim 16, Maeng et al. disclose in Fig. 11, the PCBs (154) and the motherboard (162) can be reconnected after being separated (via socket 164).

As to claim 17, Maeng et al. disclose in Fig. 11, the motherboard (162) is not damaged when the PCBs (154) are separated therefrom (via socket 164).

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Voss et al. (u.s.p 6,750,646) related to the Apparatus for environmental testing of a device in situ,and method thereof.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
12/07/04

DAVID ZARNEKE
PRIMARY EXAMINER
12/9/04